Bishop Brock

12306 McCurry Road Coupland, Texas 78615
(512) 281-3928 [Home/Office] (512) 818-0822 [Cell]
bcb@tsyvery.com

Education

M.S. in Computer Sciences, *The University of Texas at Austin*, December 1987. Advisor: W. W. Bledsoe. Research topic: Theorem proving by analogy.

B.S. in Chemistry with Honors, **B.A. with Honors** (Computer Sciences), *The University of Texas at Austin*, May 1979. Advisor: John C. Gilbert. Research topic: Synthesis and physical chemistry of metheylenecyclopropanes.

Professional Experience

Private Trader and Developer, Coupland, Texas, September 2004 to present.

Trading electronic futures markets using privately developed distributed, real-time trade execution and market analysis systems.

Research Staff Member, *IBM Research***,** Austin, Texas, August 1997 to August 2004.

Member of two internally award-winning research projects: The IBM PowerPC 405LP and the design of a NUMA server based on standard IA32 systems. Embedded system hardware and software design and power management; scalable system performance monitoring hardware and software; Linux systems programming; logic design; RTOS design; hardware and software emulation of new designs; graphical simulation interfaces; project management.

Computing Research Scientist, *Computational Logic, Inc*., Austin, Texas, October 1993 to May 1996 and January 1988 to July 1991.

Successfully completed two significant academic research programs on the application of automated reasoning to hardware and software verification problems: the FM9001 microprocessor and the Motorola CAP DSP processor. Developed and enhanced automated reasoning techniques.

Member of the Technical Staff, *Microelectronics and Computer Technology Consortium (MCC)***,** Austin, Texas, June 1986 to August 1987 and January 1985 to January 1986.

Research in theorem proving by analogy; hardware design language and circuit partitioning systems; novel logic simulation techniques.

Senior Engineer, *CALMA Company* (and predecessors), Austin, Texas and London, England, November 1979 to August 1984.

Research, development, development management and support of digital logic, timing and fault simulation products.

Skills, Knowledge and Experience

- **Software, Languages and Systems**

  Fluent**:** C, Tcl/Tk/Itcl/Iwidgets/BLT, LISP, PowerPC architecture and assembler.

  Well-versed**:** C++, UNIX systems programming, Linux kernel and driver programming, object-oriented design and programming, GUI development and usability issues, distributed systems using TCP/IP, modern computer architecture, real-time operating systems and programming, operating systems internals, TradeStation EasyLanguage and DLL API, Interactive Brokers TWS API**,** French**.**

  Exposure**:** Java and its native interface, Perl, Prolog, Microsoft Windows systems programming, Microsoft VBA, SQL, DSP architecture.

- **Hardware Design**

  Fluent: High-speed FPGA design, synthesizable VHDL for synchronous designs, PCI hardware and software design, dynamic power management support.

  Well-versed: Embedded processor and network processor board design issues and bring-up, design verification and fault simulation tools.

  Exposure: Schematic capture and board design tools, timing closure for digital designs.

- **Formal Methods and Automated Reasoning**

  Fluent: Formal specification and proof-based verification of hardware and software using ACL2 and NQTHM.

  Well-versed: Mechanization of first-order logic, resolution provers.

  Exposure: Decision procedure-based formal methods.

Honors and Awards

IBM Research Division Award, *Design of the Earl Ultra-Low-Power System-on-a-Chip*, May 2002.

IBM Invention Achievement Award, *Third Plateau* (12 patent applications), November 2001.

IBM Research Division Technical Group Award, *NUMA Server Based on SHV IA32 Systems*, January 2000.

Robert A. Welch Scholar and Welch Undergraduate Research Scholar, *The University of Texas at Austin*, 1975 to 1979.

Articles in Technical Journals

1. Brock, B., Kaufmann, M., and Moore, J, "Rewriting with Equivalence Relations in ACL2", to appear in *Journal of Automated Reasoning*.

2. Nowka, K., Carpenter, G. and Brock, B., "The Design and Application of the PowerPC 405LP Energy-Efficient System-on-a-Chip", *IBM J. Res. & Dev*., **47** (5/6), September/November 2003, pp. 631-639.

3. Nowka, K. *et al*., "A 32-bit PowerPC System-on-a-chip with Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling", *IEEE Journal of Solid-State Circuits*, **37** (11), November 2002, pp. 1441-1447.

4. Brock, B. *et al*., "Experience with Building a Commodity Intel-based ccNUMA System", *IBM J. Res. & Dev*., **45** (2), March 2001, pp. 207-227.

5. Brock, B. and Hunt, W. A., Jr., "The Dual-Eval Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor", *Formal Methods in System Design,* **11** (1), July 1997, pp. 71-104.

6. Hunt, W. A., Jr. and Brock, B., ``A Formal HDL and its Use in the FM9001 Verification'', *Philosophical Transactions of the Royal Society: Physical and Engineering Sciences,* **339** (1652), April 1992, pp. 35-47.

Articles in Technical Conference Proceedings

7. Brock, B. and Rajamani, K, "Dynamic Power Management for Embedded Systems", *Proceedings of the IEEE International SOC Conference, 2003*, September 2003, pp. 416-419.

8. Brock, B. *et al*., ``Windows NT in a ccNUMA System", *Proceedings of the 3rd USENIX Windows NT Symposium*, Seattle, Washington, July 1999.

9. Brock, C. (sic) and Hunt, W. A., Jr., "Formally Specifying and Mechanically Verifying Programs for the Motorola Complex Arithmetic Processor DSP", *Proceeding of the 1997 IEEE International Conference on Computer Design (ICCD '97)*, IEEE, 1997, p. 31-36.

10. Brock, B., Kaufmann, M. and Moore, J, ``ACL2 Theorems about Commercial Microprocessors", *Formal Methods in Computer-Aided Design (Proceedings of FMCAD '96),* Lecture Notes in Computer Science, **1166**, Srivas, M. and Camilleri, A. (Eds.), Springer, 1996, pp 275-293.

11. Brock, B., Hunt, W. A., Jr., and Young, W. D., "Introduction to a Formally Defined Hardware Description Language", *Proceedings of the IFIP TC10/WG 10.2 international Conference on Theorem Provers in Circuit Design: Theory, Practice and Experience,* V. Stavridou, V., Melham, T. and Boute, R. (Eds.), IFIP Transactions, **A-10**, North-Holland, 1992, pp. 3-35.

12. Brock, B. and Hunt, W. A., Jr., ``Report on the Formal Specification and Partial Verification of the VIPER Microprocessor", *Proceedings of the Sixth Annual Conference on Computer Assurance (COMPASS 1991)*, IEEE, June 1991, pp. 91-98.

13. Brock, B., and Hunt, W. A., Jr., "The Formalization of a Simple Hardware Description Language", *Proceedings of the IFIP TC10/WG 10.2/WG 10.5 International Workshop on Applied Formal Methods for Correct VLSI Design,* Claesen, L. (Ed.), Formal VLSI Specification and Synthesis, VLSI Design Methods-I, North-Holland, 1990, pp. 83-98.

14. Hunt, W. A., Jr., and Brock, B., "The Verification of a Bit-Slice ALU", *Hardware Specification, Verification and Synthesis: Mathematical Aspects*, Leeser, M. and Brown, G. (Eds.), Lecture Notes in Computer Science **408**, Springer, 1990, pp. 282-306.

15. Brock, B., Cooper, S. and Pierce, W., ``Analogical Reasoning and Proof Discovery", *Proceedings of the 9th International Conference on Automated Deduction,* Lusk, E. and Overbeek, R. (Eds.), Lecture Notes in Computer Science, **310**, Springer, 1988, pp. 454-468.

16. Smith, S., Mercer, M. and Brock, B., ``Demand-Driven Simulation: BACKSIM", *Proceedings of the 24th Design Automation Conference*, IEEE, June 1987, pp. 181-187.

Book Chapters

17. Moore, J and Brock, B., "A Mechanically Checked Proof of a Comparator Sort Algorithm", in Broy, M., Gruenbauer, J., Harel, D. and Hoare, T. (Eds.), *Engineering Theories of Software Intensive Systems*, Springer NATO Science Series II, **195**, Springer, 2005, pp. 141-175.

18. Brock, B. and Hunt, W. A., Jr., ``Formal Analysis of the Motorola CAP DSP", *Industrial-Strength Formal Methods in Practice*, Hinchey, M. and Bowen, J. (Eds.), Springer, 1999, pp. 81-116.

19. Brock, B. and Hunt, W. A., Jr., "A Formal Introduction to a Simple HDL", *Formal Methods for VLSI Design*, Staunstrup, J. (Ed.), IFIP WG 10.5 Lecture Notes, North-Holland, 1990, pp. 285-327.

Selected Proprietary Technical Publications

20. Supporting documents: http://www.tsyvery.com/bishop/resume.

21. Olsen, C. M. *et al*., *Analysis of Transition Energy and Latency of the PowerDown State in Advanced System-on-a-Chip Processors*, IBM Research Technical Report **RC22970**, 2003. Reprints are available upon request.

22. *Dynamic Power Management for Embedded Systems*, IBM and MontaVista Software Whitepaper, November 2002. http://www.mvista.com/downloads/wp_power_management.pdf

23. Brock, B., Hunt, W. A., Jr. and Kaufmann, M., *The FM9001 Microprocessor Proof*, Computational Logic, Inc., Technical Report **86**, December 1994. http://www.computationallogic.com/reports/files/086.ps.

24. Brock, B., *An "Improved" Clausifier for NQTHM*, Computational Logic, Inc., Note **128**, June 1989. Reprints are available upon request.

25. Brock, B., *An Experimental Implementation of Equivalence Reasoning in the Boyer-Moore Theorem Prover*, Computational Logic, Inc., Note **104**, January 1989. Reprints are available upon request.

Invited Presentations

26. Invited Paper: *Dynamic Power Management for Embedded Systems*, IEEE International SOC Conference, September 2003.

27. Invited Panelist: *Linux Power Management for Consumer Devices*, Consumer Electronics Show, Las Vegas, Nevada, January 2004.

28. Invited Lecture: *Hardware Verification using an HDL*, Summer School on Formal Methods for VLSI Design, Technical University of Denmark, Lyngby, Denmark, June 1990.

US Patents (All as Co-Inventor; All assigned to IBM)

29. **US6886106**: *System and Method for Controlling a Multiplexer for Selecting Between an Input Clock and an Input Duty-Cycle-Corrected Clock and Outputting the Selected Clock and an Enable Signal*, April 2006.

30. **US6836849**: *Method and Apparatus for Controlling Power and Performance in a Multiprocessing System According to Customer Level Operational Requirements*, December 2004.

31. **US6662251**: *Selective Targeting of Transactions to Devices on a Shared Bus,* December 2003.

32. **US6601149**: *Memory Transaction Monitoring System and User Interface*, July 2003.

33. **US6499028**: *Efficient Identification of Candidate Pages and Dynamic Response in a NUMA Computer*, December 2002.

34. **US6473085**: *System for Dynamically Adjusting Image Quality for Interactive Graphics Applications*, October 2002.

35. **US6442654**: *Operating System Support for In-Server Caching of Documents*, August 2002.

36. **US6421775**: *Interconnected Processing Nodes Configurable as at least one Non-Uniform Memory Access (NUMA) Data Processing System*, July 2002.

37. **US6349394**: *Performance Monitoring in a NUMA Computer*, February 2002.