Bishop Brock

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Qualifications

During my career I have had the opportunity to contribute to several computing disciplines including high-performance computational finance [1], large-system verification, validation and power management [2,4,6,7,8,38,41,42], embedded systems design and power management [14,15,48], large-system architecture and performance analysis [20,53,54], automated reasoning [12,33,35], formal verification of hardware and software [13,25,27] and electronic design automation [36].

As a computer system designer and developer my experience ranges from FPGA logic [20] up to complete embedded computer systems [70]. In many cases I also developed the application or operating environment software required for research or deployment of the systems. I have led the development of full-system simulation infrastructures to support both large-system power management [4] and specialized embedded applications [2]. Recent work also includes embedded processor architectures, RTOS [66] and ecosystems [42] for embedded environments targeting current and future IBM POWER systems.

In addition to authoring technical publications I am also the co-inventor of eighteen US patents, and was honored to be named an IBM Master Inventor in 2015.

My background in formal methods provides a unique perspective on software and system design, founded on rigorous reasoning about specification and correctness issues.

Professional Experience

Research Staff Member, *IBM Research*, Austin, Texas, September 2014 to present.

I am an active contributor to the Hyperledger fabric [64], an open-source implementation of a permissioned blockchain. I contributed the busywork exerciser framework to the fabric, and I am currently investigating high-performance distributed consensus methodologies in the context of the next-generation fabric architecture.

My first project on rejoining IBM Research in 2014 was to lead the development of a STAC-A2™ benchmark solution for POWER8 systems [65]. Frank Liu and I were able to demonstrate record-setting performance and scalability on this financial risk analytics workload, and together with Karthick Rajamani we also reported on novel algorithms and performance analysis related to the benchmark [1]. Following this work my focus area was Apache Spark, and the potential for various types of hardware acceleration for Spark workloads.

Senior Scientist, *IBM Systems and Technology Group*, Austin, Texas, April 2008 to August 2014.

After rejoining IBM in 2008 I began work in a group dedicated to POWER microprocessor power management. My final projects in this organization included the development of a new embedded processor architecture, power management firmware, full-system simulation infrastructure and other tools (including a novel tool for code-coverage analysis), all targeting future POWER9 systems. For POWER9 we elected to replace the proprietary micro-sequencers used in POWER8 (see below) with a new microarchitecture based on the embedded Power ISA specification. Michael Floyd and I architected a small, fast embedded microcontroller that will be used extensively throughout the

Professional Experience (Cont.)

POWER9 chip. Although this tiny machine is not fully Power ISA compliant, it still supports C/C++ compilation with slightly modified Power ISA tool chains.

With POWER8 the external power management controller of POWER7 systems was brought on-chip as a PowerPC 405 core, assisted by several small proprietary micro-sequencers. The PowerPC 405 core, known as the On-Chip Controller (OCC), runs a proprietary RTOS (SSX, [66]) that I architected and developed. For POWER8 I also lead teams developing system-level simulation of power management and other functions, and specialized ecosystems for developing applications for these processors. In particular we developed a powerful technique for debugging and analysis of assembly language programs using high-level language annotations [2,42], as well as a new embedded scripting language. I architected and implemented bring-up and product applications both for the OCC and proprietary micro-sequencers, along with continuing the Virtual Power Management (VPM) and bring-up infrastructure work started with POWER7 (see below).

My earlier work on POWER7 included architecting and implementing new system-level verification and validation tools and strategies for POWER7 power management functions, including tools to improve productivity in the development of complex laboratory test and analysis procedures. One component of this work is an efficient event-driven verification methodology for hardware-accelerated simulation of power management logic [8]. Another component is a new system-level power modeling approach, *Virtual Power Management* (VPM) [4], which allows standalone architectural evaluation as well as end-to-end product firmware development and benchmarking with realistic power and performance models for large server systems. The VPM tool has been used to analyze proposed power management architectures for POWER7+ and POWER8 systems, and both the verification and validation approaches are now mainstream within IBM POWER systems development.

As part of the POWER7 delivery effort I was a member of a team that demonstrated how Critical Path Monitors (CPM) could be used to significantly reduce server energy consumption without sacrificing performance [6,44], as well as a member of a team exploring techniques to estimate power consumption of server processors using hardware event monitors [5].

Private Trader and Developer, Coupland, Texas, September 2004 to March 2008.

During this period, I traded commodity futures for my private account. This work included the development of a distributed, real-time trading platform including market analysis applications and automated execution heuristics.

Research Staff Member, *IBM Research*, Austin, Texas, August 1997 to August 2004.

I was a member of an IBM Austin Research Laboratory (ARL) team that designed and delivered an ultra-low-power embedded processor, the IBM PowerPC 405LP [14]. This research program anticipated devices like the Apple iPhone, that is, high-function consumer devices requiring well-managed power consumption over a wide range of application performance points. After leading the team that developed Linux support for the new capabilities of the processor, I then focused my research on software-controlled power management, especially latency optimization and applications of dynamic voltage and frequency scaling [15]. However, I also contributed to and supported many aspects of the project including the specification of the 405LP's standby power management controller, specification of a dynamic power management protocol for embedded Linux [18], consulting on 405LP reference designs, optimizing video applications, customer engagement and technology transfer for the commercial follow-on product. As a member of ARL I contributed to power management research spanning a wide range of system configurations [16,47].

Professional Experience (Cont.)

Earlier, I was a member of another ARL team that assembled a 16-processor cache-coherent non-uniform memory access (NUMA) system based on 4-processor Intel Xeon servers [20,53]. David Glasco and I designed an interface board that integrated third-party cache coherence and high-speed interconnect logic with a proprietary performance monitoring function. I designed both the hardware (high-speed FPGA) and software (Linux device driver) for the performance monitor, and implemented novel performance monitoring utilities [49,54]. The Linux driver includes a software emulation of the performance monitor function which allowed application development to proceed before the hardware was available.

While at ARL I also designed two special-purpose single-board computers in furtherance of our research on dense servers. The *Pecan* board featured a PowerPC 405GP on a PCI card along with an FPGA for custom logic. Originally designed as a prototype for a low-power network appliance or dense server, a software team under my direction used a cluster of *Pecan* boards to emulate the PowerPC 405LP (implementing new hardware components in the FPGA), allowing us to develop much of the Linux support for the 405LP prior to delivery of the first prototype hardware. Pecan was also used for power experiments by a number of other researchers [69]. Two colleagues and I also designed an experimental, power-efficient network caching appliance for dense installations dubbed *Singularity*. *Singularity* is a Compact PCI card featuring a cluster of 8 PowerNP NPe405L processors backing a PowerNP NP4GS3 network processor. Preliminary work on the *Singularity* design led to advances in hardware cluster security [48].

In support of our embedded systems work I designed and developed a real-mode RTOS for embedded PowerPC processors that was used in several of our projects. A derivative of this RTOS ships in IBM POWER8 systems (SSX, see above), and is currently in-plan for POWER9 as well.

My final project at ARL involved the design of test logic for the test chip of an experimental circuit family. The test logic included a programmable array tester using cellular automata-based pseudo-random pattern generators and systolic decrementers, and was exercised via a custom graphical 'test harness' I developed for the IBM logic simulation system. The test harness design allowed the same interface to be used both for logic simulation as well as for testing of the actual device.

Computing Research Scientist, *Computational Logic, Inc.*, Austin, Texas, October 1993 to May 1996 and January 1988 to July 1991.

At Computational Logic, Inc. I completed two successful research programs on the applications of automated reasoning to hardware and software verification problems. This research is notable in terms of the techniques used, the completeness of the analysis and/or the complexity of the systems studied.

Together with two others I formally specified the Motorola Complex Arithmetic Processor (CAP) DSP using ACL2 [22]. The CAP was indeed a complex processor, with numerous parallel addressing and execution units, and a pipeline containing exposed hazards. I next obtained a mechanical proof of equivalence of the actual, pipelined implementation of the CAP with a simpler, sequential execution model of the processor. This proof is interesting in that it required formalizing the set of programs which do not expose the inherent pipeline hazards, as these are the only programs that are executed equivalently by the two formal models. Finally, the sequential execution model was used to obtain mechanical proofs of correctness of two firmware applications [24]. I was also responsible for the day-to-day management of the research contract. Parts of this work involved a technique known as *congruence reasoning*, whose prototype implementation I had originally developed in the context of the Boyer-Moore theorem prover NQTHM [12,34]. Libraries of definitions and lemmas I developed during this project are distributed with ACL2.

Professional Experience (Cont.)

Earlier, Warren Hunt I developed a formal, hierarchical, gate-level hardware design language (HDL) named DUAL-EVAL [23]. The syntax of DUAL-EVAL was a small step away from commercial HDLs of the period, and the execution semantics of DUAL-EVAL were provided by an interpreter in NQTHM. We then specified, designed and mechanically verified the 32-bit FM9001 microprocessor, using DUAL-EVAL and NQTHM [26]. The use of DUAL-EVAL was a significant step because formal hardware verification as typically practiced involves models that are not formally connected to actual design data, whereas our DUAL-EVAL netlist for the FM9001 was both low-level design data as well as a formal mathematical object. Also new in this work was the fact that we did not simply verify static netlists, but we also verified functions that *created* netlists for certain types of parameterized hardware circuits. The processor was eventually fabricated as a gate array from the verified gate-level netlist. This exercise demonstrated the feasibility of verifying a processor from a high-level specification to a low-level design within the same formal system. In support of this work I designed an improved propositional simplification procedure for NQTHM which was essential for the success of the project [33].

Member of the Technical Staff, *Microelectronics and Computer Technology Consortium (MCC)***,** Austin, Texas, June 1986 to August 1987 and January 1985 to January 1986.

During my graduate studies I worked at MCC both in the Artificial Intelligence Program and in the VLSI CAD program. In the Artificial Intelligence program my colleagues and I implemented an automated theorem prover which used the proofs of previously proven theorems to guide the proofs of new, analogous theorems [35]. This was a resolution prover geared towards proofs in elementary analysis.

While in the VLSI CAD program I developed a design language system and a circuit partitioning system for the program. Steve Smith and I also jointly invented a new logic simulation technique, *demand-driven simulation* [36].

Senior Engineer, *CALMA Company* (and predecessors), Austin, Texas and London, England, November 1979 to August 1984.

I began my career maintaining, installing and porting an early commercial logic, timing and fault simulation system named TEGAS. I eventually led a small group that developed and shipped TEXSIM, the first commercial design verification simulator to include a model of media (wire) delays. I also produced prototype implementations of new design verification and fault simulators, including a multi-word parallel fault simulator prototype which was later developed and marketed. I spent most of 1983 on assignment in London, England, providing customer support for simulation products at our newly-established European office.

Education

M.S. in Computer Sciences, *The University of Texas at Austin*, December 1987. Advisor: W. W. Bledsoe. Research topic: Theorem proving by analogy [35].

B.S. in Chemistry with Honors, **B.A. with Honors** (Computer Sciences), *The University of Texas at Austin*, May 1979. Undergraduate research advisor: John C. Gilbert. Research topic: Synthesis and physical chemistry of metheylenecyclopropanes.

Skills and Experience

- **Software, Languages and Systems**

  Fluent**:** C; Tcl/Tk/Itcl/Iwidgets/BLT; LISP; PowerPC architecture and assembler; Dynamic power management from embedded systems to commercial servers; RTOS.

  Well-versed**:** C++; Python; Go and the Go runtime implementation; Full-system simulation including Wind River Simics; UNIX systems programming; Linux kernel and driver programming; GUI development and usability issues; Distributed systems using TCP/IP; Modern computer architecture, Operating systems internals; French**.**

  Exposure**:** Apache Spark; Scala; Ruby; Rails; Code-coverage analysis; Java and its native interface; Perl; Prolog; FORTRAN; Microsoft Windows systems programming; Microsoft VBA.

- **Hardware Design and Verification**

  Fluent: Embedded processor architecture; High-speed FPGA design, synthesizable VHDL for synchronous designs, dynamic power management support.

  Well-versed: Large-systems pre- and post-silicon bring-up; Embedded processor and network processor board design issues and bring-up; Functional verification, design verification and fault simulation tools.

  Exposure: Hardware verification metrics; Schematic capture and board design tools.

- **Formal Methods and Automated Reasoning**

  Fluent: Formal specification and proof-based verification of hardware and software using ACL2 and NQTHM.

  Exposure: Decision procedure-based formal methods.

Other Experiences

My graduate studies spanned the period from fall 1984 to summer 1987. Besides working at MCC, I also enjoyed three semesters as a teaching assistant for undergraduate programming classes. From fall 1991 through spring 1993 I traveled approximately 12,500 miles by bicycle in eleven countries on four continents, fulfilling a goal I had set after cycling coast-to-coast a few years earlier. The period from summer 1996 through summer 1997 was also devoted to world travel, including long cycling tours, mountaineering and trekking.

Publications

1. Brock B., Liu, F. and Rajamani, K., "STAC-A2™ Benchmark on POWER8", *Workshop on High-Performance Computational Finance (WHPCF'15)*, November 20, 2015.

2. Schubert, K., Ludden, J., Ayub, S., Behrend, J., Brock, B., Copty, F., German, S. M., Horbach, H., Jackson, J. R., Keuerleber, K., Koesters, J., Leitner, L. S., Meil, G. B., Meissner, C., Morad, R., Nahir, A., Paruthi, V., Peterson, R. D., Pratt R. R., Rimon, M. and Schumann, J., "Solutions to POWER8 Verification Challenges", *IBM J. Res. & Dev.*, **59(**1), January/February 2015, pp. 11:1-11:17.

3. Lefurgy, C., Drake, A. J., Floyd, M., Allen-Ware, M., Brock, B., Tierno, J. A., and Carter, J. B., "Active Guardband Management in POWER7+ to Save Energy While Maintaining Reliability and Performance", *IEEE Micro,* **33**(4), July/August 2013, pp. 35-45.

4. Brock, B., Ramani, S., Hanson, H., Vu, K. and Floyd, M., "Virtual Power Management Simulation Framework for Computer Systems*", Proceedings of the 2013 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS),* April 2013, pp. 128-129.

5. Huang, W., Kuk, W., Floyd, M., Buyuktosunoglu, A., Lefurgy, C., Allen-Ware, M., Brock, B. and Rajamani, K., "Accurate Fine-Grained Processor Power Proxies", *Proceedings of the 2012 45th Annual IEEE/ACM International Symposium on Microarchitecture* (MICRO-45), December 2012, pp. 224-234.

6. Lefurgy, C., Drake, A. J., Floyd, M. S., Allen-Ware, M., Brock, B., Tierno, J. A., and Carter, J. B., "Active Management of Timing Guardband to Save Energy in POWER7", *Proceeding of the 44th Annual IEEE/ACM International Symposium on Microarchitecture* (MICRO 2011), December 2011, pp. 1-11.

7. Floyd, M., Ware, M., Rajamani, K., Gloekler, T., Brock, B., Bose, P., Buyuktosunoglu, A., Rubio, J. C., Schubert, B., Spruth, B., Tierno, J. A. and Pesantez, L.*, "*Adaptive energy-management features of the IBM POWER7 chip", *IBM J. Res. & Dev.*, **55** (3), May/June 2011, pp. 8:1 – 8:18.

8. Schubert, K.-D., Roesner, W., Ludden, J. M., Jackson, J., Buchert, J., Paruthi, V., Behm, M., Ziv, A., Schumann, J., Meissner, C., Koesters, J., Hsu, J. and Brock, B., "Functional verification of the IBM POWER7 microprocessor and POWER7 multiprocessor systems", *IBM J. Res. & Dev.*, 55 (3) May/June 2011, pp. 10:1 – 10:17.

9. Floyd, M., Ware, M., Rajamani, K., Brock, B., Lefurgy, C., Drake, A. J., Pesantez, L., Gloekler, T., Tierno, J. A., Bose, P. and Buyuktosunoglu, A., "Introducing the Adaptive Energy Management Features of the POWER7 Chip", *IEEE Micro*, **31** (2), pp. 60-75.

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11. Ware, M., Rajamani, K., Floyd, M., Brock, B., Rubio, J. C., Rawson, F. and Carter J. B, "Architecting for power management: The IBM POWER7", *Proceedings of the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2010),* January 2010, pp. 1-11.

12. Brock, B., Kaufmann, M., and Moore, J, "Rewriting with Equivalence Relations in ACL2", *Journal of Automated Reasoning,* **40** (4), May 2008, pp. 293-306.

13. Moore, J and Brock, B., "A Mechanically Checked Proof of a Comparator Sort Algorithm", in Broy, M., Gruenbauer, J., Harel, D. and Hoare, T. (Eds.), *Engineering Theories of Software Intensive Systems*, Springer NATO Science Series II, **195**, Springer, 2005, pp. 141-175.

14. Nowka, K., Carpenter, G. and Brock, B., "The Design and Application of the PowerPC 405LP Energy-Efficient System-on-a-Chip", *IBM J. Res. & Dev*., **47** (5/6), September/November 2003, pp. 631-639.

15. Brock, B. and Rajamani, K, "Dynamic Power Management for Embedded Systems", *Proceedings of the IEEE International SOC Conference, 2003*, September 2003, pp. 416-419.

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22. Brock, B. and Hunt, W. A., Jr., ``Formal Analysis of the Motorola CAP DSP", *Industrial-Strength Formal Methods in Practice*, Hinchey, M. and Bowen, J. (Eds.), Springer, 1999, pp. 81-116.

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23. Brock, B. and Hunt, W. A., Jr., "The Dual-Eval Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor", *Formal Methods in System Design,* **11** (1), July 1997, pp. 71-104.

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33. Brock, B., *An "Improved" Clausifier for NQTHM*, Computational Logic, Inc., Note **128**, June 1989. Reprints are available from the author.

34. Brock, B., *An Experimental Implementation of Equivalence Reasoning in the Boyer-Moore Theorem Prover*, Computational Logic, Inc., Note **104**, January 1989. Reprints are available from the author.

35. Brock, B., Cooper, S. and Pierce, W., ``Analogical Reasoning and Proof Discovery", *Proceedings of the 9th International Conference on Automated Deduction,* Lusk, E. and Overbeek, R. (Eds.), Lecture Notes in Computer Science, **310**, Springer, 1988, pp. 454-468.

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36. Smith, S., Mercer, M. and Brock, B., ``Demand-Driven Simulation: BACKSIM'', *Proceedings of the 24th Design Automation Conference*, IEEE, June 1987, pp. 181-187.

US Patents (all as Co-Inventor)

37. **US9372717:** *Interruption of Chip Component Managing Tasks*, June 2016.

38. **US9323300:** *Computing System Voltage Control*, April 2016.

39. **US9304886:** *Associating Energy Consumption with a Virtual Machine*, April 2016**.**

40. **US9218044:** *Computing System Frequency Target Monitor*, December 2015.

41. **US9182797:** *Decoupled Power and Performance Allocation in a Multiprocessor System,* November 2015.

42. **US9134966:** *Management of Mixed Programming Languages for a Simulation Environment,* September 2015.

43. **US8635483**: *Dynamically Tune Power Proxy Architectures*, January 2014.

44. **US8527801:** *Performance Control of Frequency-Adapting Processors by Voltage Domain Adjustment,* September 2013.

45. **US8370517:** *Conserving Energy in a Data Processing Network,* February 2013.

46. **US6886106**: *System and Method for Controlling a Multiplexer for Selecting Between an Input Clock and an Input Duty-Cycle-Corrected Clock and Outputting the Selected Clock and an Enable Signal*, April 2006.

47. **US6836849**: *Method and Apparatus for Controlling Power and Performance in a Multiprocessing System According to Customer Level Operational Requirements*, December 2004.

48. **US6662251**: *Selective Targeting of Transactions to Devices on a Shared Bus,* December 2003.

49. **US6601149**: *Memory Transaction Monitoring System and User Interface*, July 2003.

50. **US6499028**: *Efficient Identification of Candidate Pages and Dynamic Response in a NUMA Computer*, December 2002.

51. **US6473085**: *System for Dynamically Adjusting Image Quality for Interactive Graphics Applications*, October 2002.

52. **US6442654**: *Operating System Support for In-Server Caching of Documents*, August 2002.

53. **US6421775**: *Interconnected Processing Nodes Configurable as at least one Non-Uniform Memory Access (NUMA) Data Processing System*, July 2002.

54. **US6349394**: *Performance Monitoring in a NUMA Computer*, February 2002.

Selected Presentations

55. Panelist: *OpenPOWER in Capital Markets*, HPC for Wall Street Conference, September 21, 2015.

56. Invited Panelist: *Linux Power Management for Consumer Devices*, Consumer Electronics Show, Las Vegas, Nevada, January 2004.

57. *Hardware Verification using an HDL*, Invited Lecture, Summer School on Formal Methods for VLSI Design, Technical University of Denmark, Lyngby, Denmark, June 1990.

Honors and Awards

58. IBM Master Inventor, December 2015.

59. IBM Invention Achievement Award, *Fifth Plateau* (representing 20 patent applications), December 2012.

60. Our MICRO-2011 paper [6] was awarded Best Paper at the conference, and also received an IBM Research Pat Goldberg Best Paper Award for 2011.

61. IBM Research Division Award, *Design of the Earl Ultra-Low-Power System-on-a-Chip*, May 2002.

62. IBM Research Division Technical Group Award, *NUMA Server Based on SHV IA32 Systems*, January 2000.

63. Robert A. Welch Scholar and Welch Undergraduate Research Scholar, *The University of Texas at Austin*, 1975 – 1979.

Supporting References

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65. POWER8 S824 STAC-A2 Audit Reports: https://stacresearch.com/IBM150305

66. SSX RTOS Source Code: https://github.com/open-power/occ/tree/master/src/ssx

67. ACL2 Homepage: http://www.cs.utexas.edu/users/moore/acl2/.

68. NQTHM homepage: ftp://ftp.cs.utexas.edu/pub/boyer/nqthm/index.html.

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